HARRIS SEMICONDUCTOR

IRFP350, IRFP351, IRFP352, IRFP353

14A and 16A, 350V and 400V, 0.3 and 0.4 Ohm, N-Channel Power MOSFETs

January 1998

Features

- 14A and 16A, 350V and 400V
- $r_{DS(ON)}$ = 0.3Ω and 0.4Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Related Literature
  - TB334 "Guidelines for Soldering Surface Mount Components to PC Boards"

Ordering Information

PART NUMBER	PACKAGE	BRAND
IRFP350	TO-247	IRFP350
IRFP351	TO-247	IRFP351
IRFP352	TO-247	IRFP352
IRFP353	TO-247	IRFP353

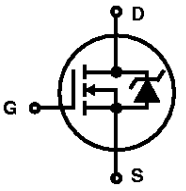
NOTE: When ordering, include the entire part number.

Description

These are N-Channel enhancement mode silicon gate power field effect transistors. They are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching convertors, motor drivers, relay drivers, and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. These types can be operated directly from integrated circuits.

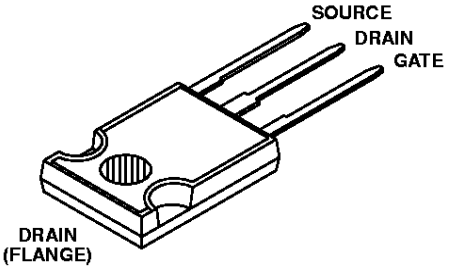
Formerly developmental type TA17434.

Symbol



Packaging

JEDEC STYLE TO-247
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

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File Number **2319.3**

Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

	IRFP350	IRFP351	IRFP352	IRFP353	UNITS
Drain to Source Voltage (Note 1) . . . . . V_{DS}	400	350	400	350	V
Drain to Gate Voltage (R_{GS} = 20kΩ) (Note 1) . . . . . V_{DGR}	400	350	400	350	V
Continuous Drain Current . . . . . I_D	16	16	14	14	A
$T_C = 100^oC$ . . . . . I_D	10	10	8.9	8.9	A
Pulsed Drain Current (Note 3) . . . . . I_{DM}	64	64	56	56	A
Gate to Source Voltage . . . . . V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation . . . . . P_D	180	180	180	180	W
Linear Derating Factor	1.44	1.44	1.44	1.44	W/^{o}C
Single Pulse Avalanche Energy Rating (Note 4) . . . . . E_{AS}	700	700	700	700	mJ
Operating and Storage Temperature . . . . . T_J, T_{STG}	-55 to 150	-55 to 150	-55 to 150	-55 to 150	^{o}C
Maximum Temperature for Soldering					
Leads at 0.063in (1.6mm) from Case for 10s . . . . . T_L	300	300	300	300	^{o}C
Package Body for 10s, See Techbrief 334 . . . . . T_{pkg}	260	260	260	260	^{o}C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

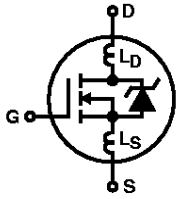
NOTE:

1. $T_J = 25^oC$ to 125^oC.

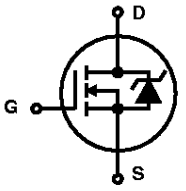
Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = 250μA, (Figure 10)				
IRFP350, IRFP352			400	-	-	V
IRFP351, IRFP353			350	-	-	V
Gate to Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, I_D = 250μA	2.0	-	4.0	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = Rated BV_{DSS}, V_{GS} = 0V	-	-	25	μA
		V_{DS} = 0.8 x Rated BV_{DSS}, V_{GS} = 0V, $T_J = 125^oC$	-	-	250	μA
On-State Drain Current (Note 2)	$I_{D(ON)}$	$V_{DS} > I_{D(ON)} \times r_{DS(ON)MAX}$, V_{GS} = 10V, (Figure 7)				
IRFP350, IRFP351			16	-	-	A
IRFP352, IRFP353			14	-	-	A
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±20V	-	-	±100	nA
Drain to Source On Resistance (Note 2)	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 8.9A, (Figures 8, 9)				
IRFP350, IRFP351			-	0.25	0.3	Ω
IRFP352, IRFP353			-	0.3	0.4	Ω
Forward Transconductance (Note 2)	g_{fs}	$V_{DS} = 2 \times V_{GS}$, I_D = 8.0A, (Figure 12)	8.0	10	-	S
Turn-On Delay Time	$t_{D(ON)}$	V_{DD} = 200V, I_D = 16A, R_G = 6.2Ω, V_{GS} = 10V, R_L = 12.3Ω, (Figures 17, 18) MOSFET Switching Times are Essentially Independent of Operating Temperature	-	12	18	ns
Rise Time	t_r		-	51	77	ns
Turn-Off Delay Time	$t_{D(OFF)}$		-	75	110	ns
Fall Time	t_f		-	47	71	ns
Total Gate Charge (Gate to Source + Gate to Drain)	Q_g	V_{GS} = 10V, I_D = 16A, V_{DS} = 0.8 x Rated BV_{DSS}, $I_{G(REF)}$ = 1.5mA, (Figures 14, 19, 20) Gate Charge is Essentially Independent of Operating Temperature	-	87	130	nC
Gate to Source Charge	Q_{gs}		-	10	-	nC
Gate to Drain "Miller" Charge	Q_{gd}		-	33	-	nC

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz, (Figure 11)		-	2000	-	pF
Output Capacitance	C_{OSS}			-	400	-	pF
Reverse-Transfer Capacitance	C_{RSS}			-	100	-	pF
Internal Drain Inductance	L_D	Measured Between the Contact Screw on Header that is Closer to Source and Gate Pins and Center of Die	Modified MOSFET Symbol Showing the Internal Devices Inductances 	-	5.0	-	nH
Internal Source Inductance	L_S	Measured From The Source Lead, 6mm (0.25in) From Header to Source Bonding Pad		-	12.5	-	nH
Junction to Case	$R_{\theta JC}$			-	-	0.70	$^oC/W$
Junction to Ambient	$R_{\theta JA}$	Free Air Operation		-	-	30	$^oC/W$

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Continuous Source to Drain Current	I_{SD}	Modified MOSFET Symbol Showing the Integral Reverse P-N Junction Diode		-	-	16	A
Pulse Source to Drain Current (Note 3)	I_{SDM}			-	-	64	A
Source to Drain Diode Voltage (Note 2)	V_{SD}	$T_J = 25^oC$, I_{SD} = 16A, V_{GS} = 0V, (Figure 13)		-	-	1.6	V
Reverse Recovery Time	t_{rr}	$T_J = 150^oC$, I_{SD} = 15A, dI_{SD}/dt = 100A/μs		270	-	1300	ns
Reverse Recovered Charge	Q_{RR}	$T_J = 150^oC$, I_{SD} = 15A, dI_{SD}/dt = 100A/μs		1.7	-	8.1	μC

NOTES:

2. Pulse Test: Pulse width ≤ 300μs, duty cycle ≤ 2%.
3. Repetitive Rating: Pulse width limited by Max junction temperature. See Transient Thermal Impedance curve (Figure 3).
4. V_{DD} = 40V, starting $T_J = 25^oC$, L = 5.66mH, R_G = 50Ω, peak I_{AS} = 15A. (Figures 15, 16).

Typical Performance Curves Unless Otherwise Specified

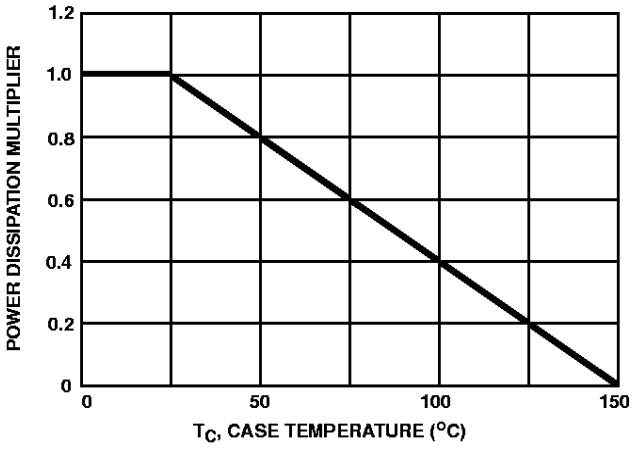


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

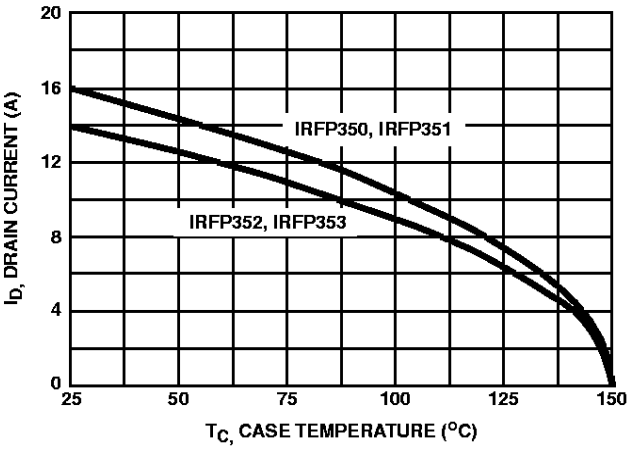


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

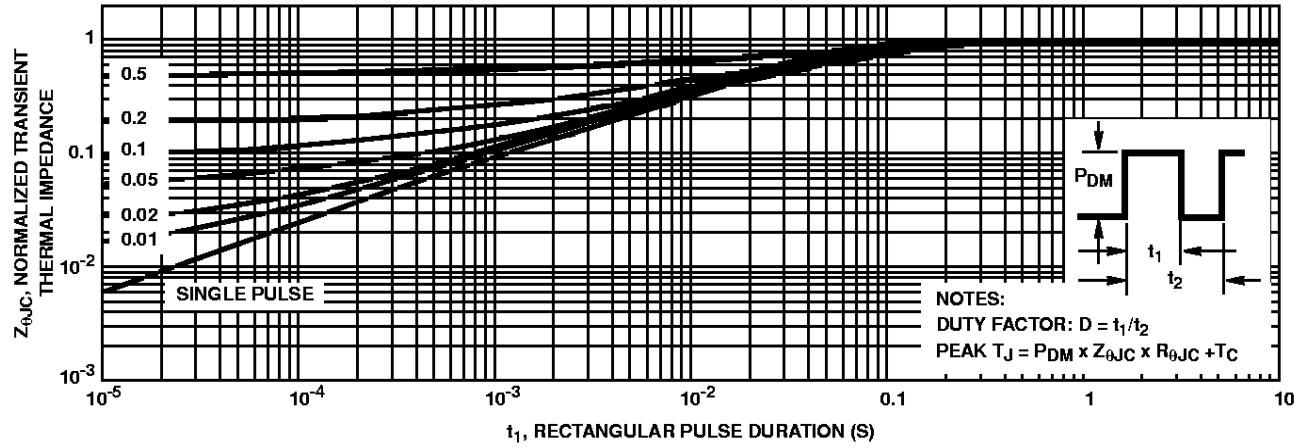


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

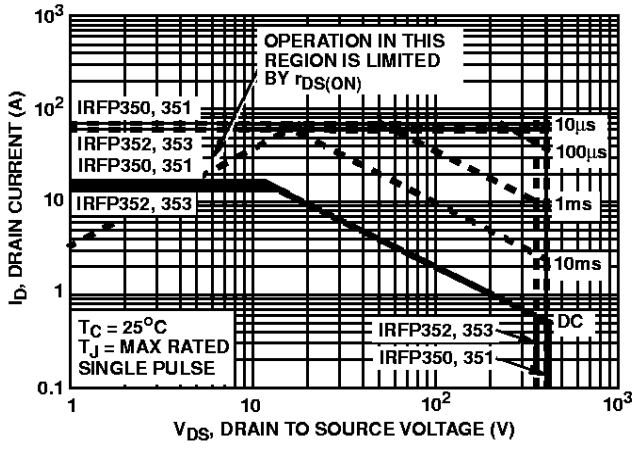


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

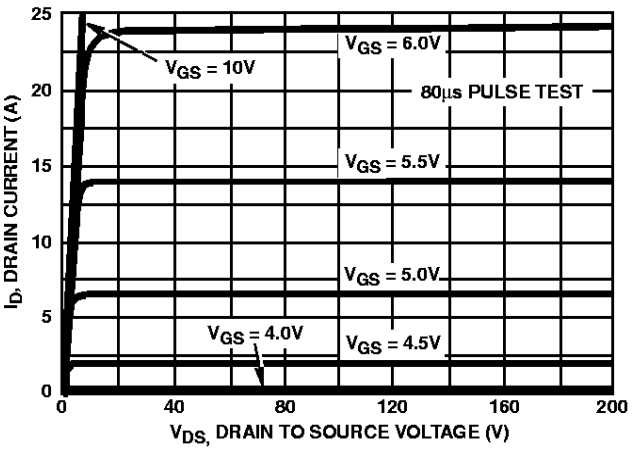


FIGURE 5. OUTPUT CHARACTERISTICS

Typical Performance Curves Unless Otherwise Specified (Continued)

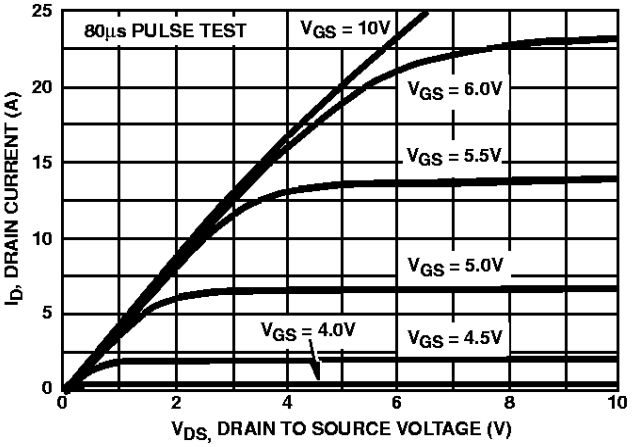


FIGURE 6. SATURATION CHARACTERISTICS

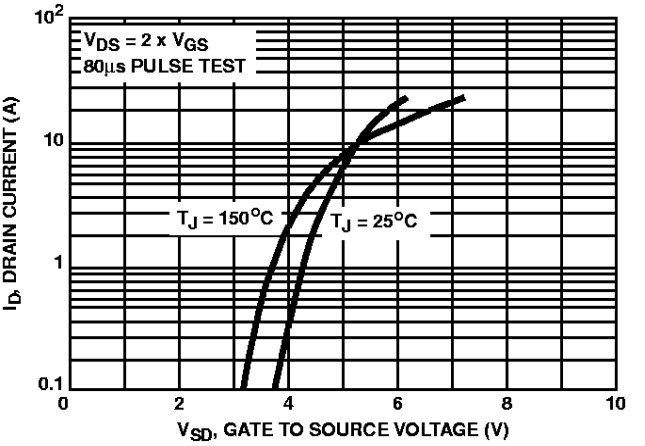


FIGURE 7. TRANSFER CHARACTERISTICS

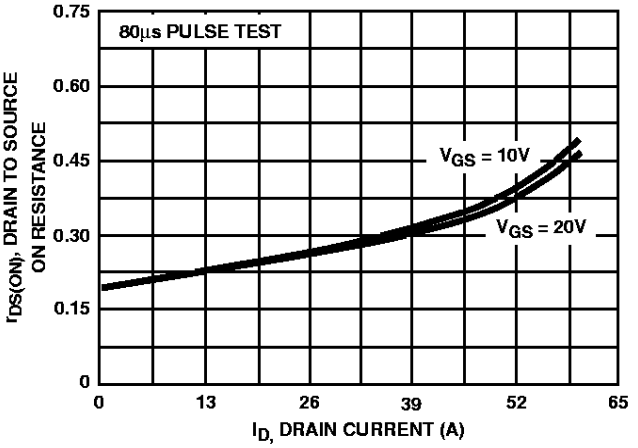


FIGURE 8. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

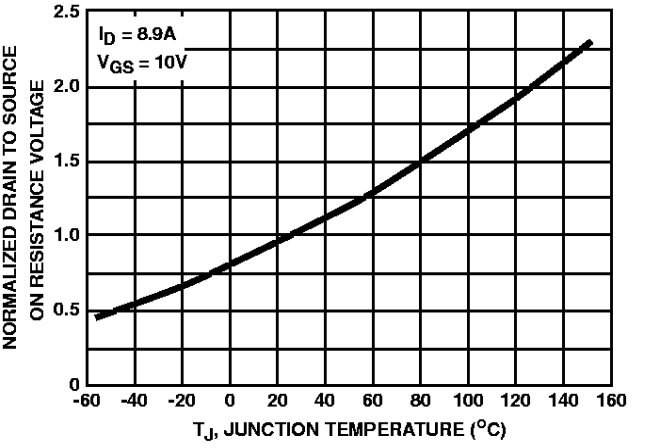


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

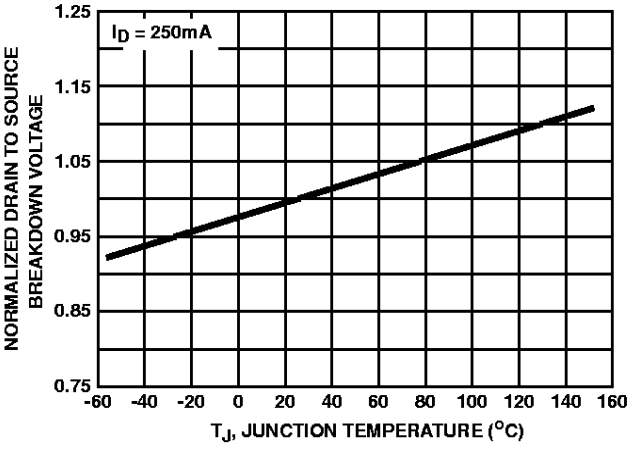


FIGURE 10. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

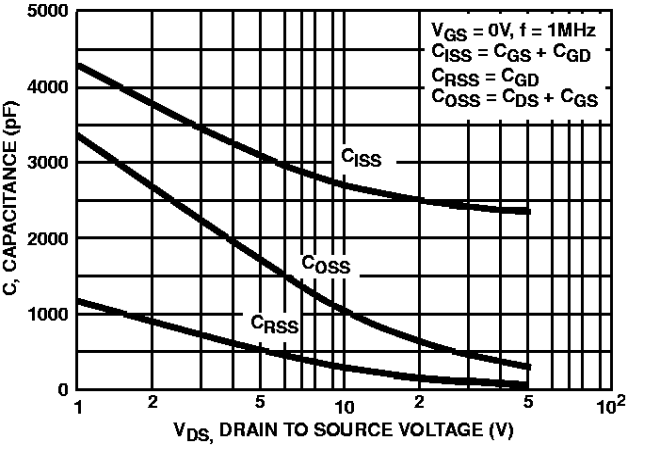


FIGURE 11. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

Typical Performance Curves Unless Otherwise Specified (Continued)

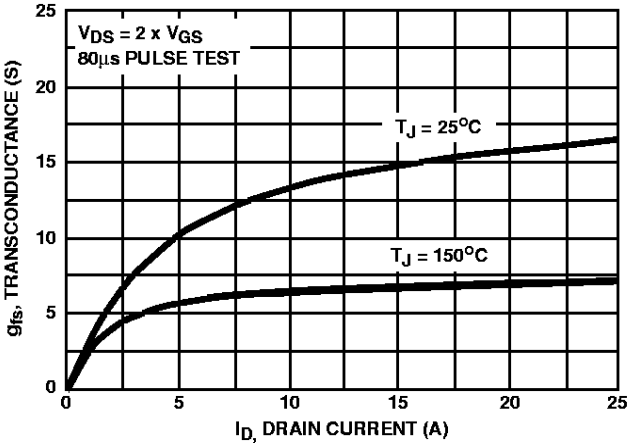


FIGURE 12. TRANSCONDUCTANCE vs DRAIN CURRENT

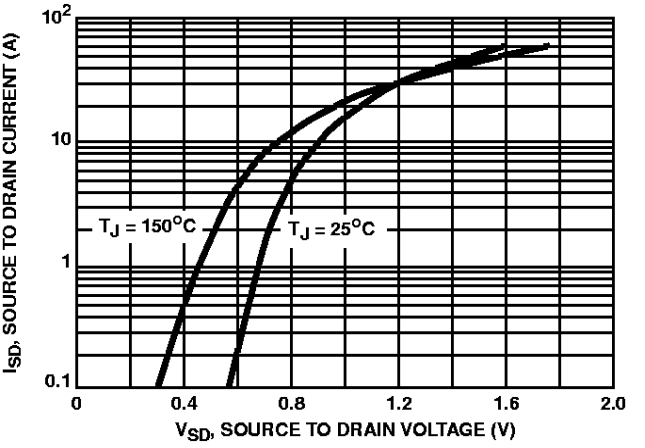


FIGURE 13. SOURCE TO DRAIN DIODE FORWARD VOLTAGE

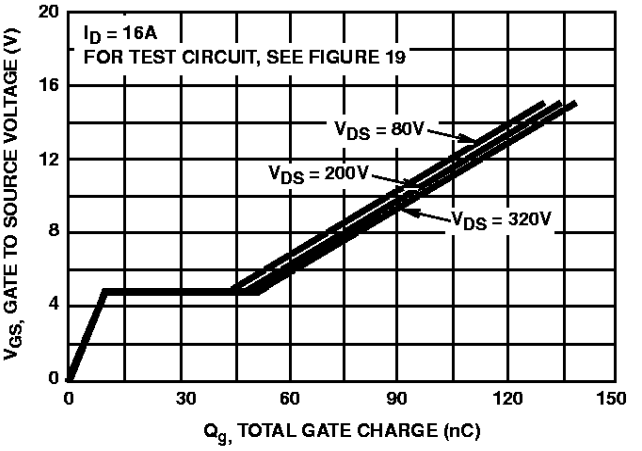


FIGURE 14. GATE TO SOURCE VOLTAGE vs GATE CHARGE

Test Circuits and Waveforms

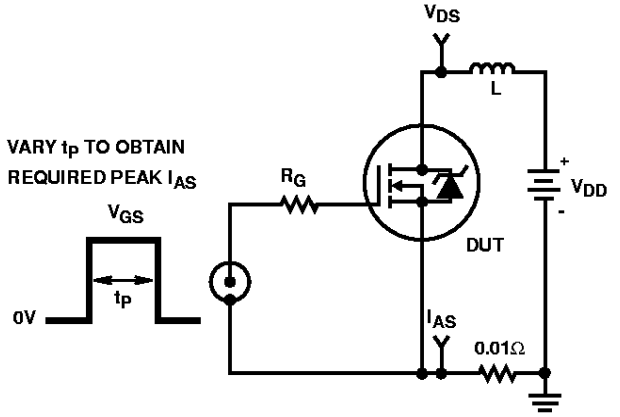


FIGURE 15. UNCLAMPED ENERGY TEST CIRCUIT

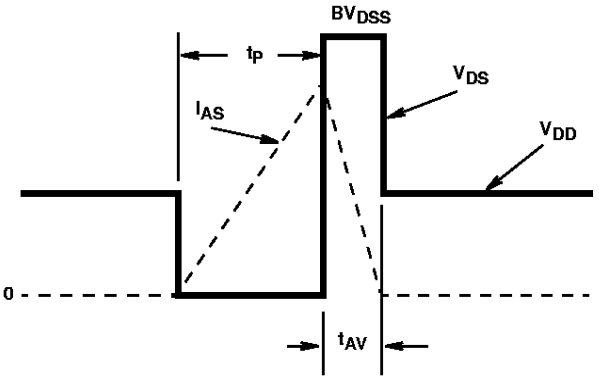


FIGURE 16. UNCLAMPED ENERGY WAVEFORMS

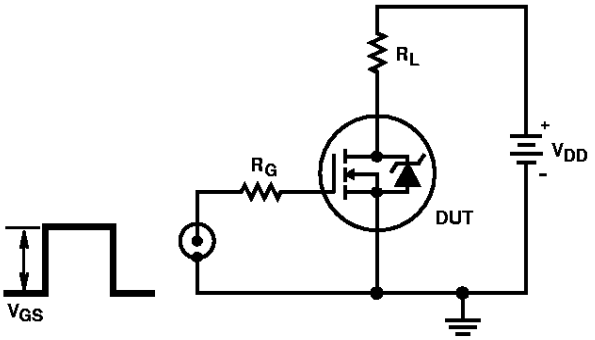


FIGURE 17. SWITCHING TIME TEST CIRCUIT

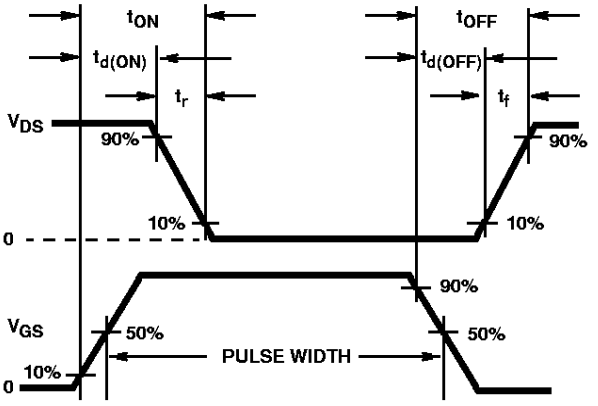


FIGURE 18. RESISTIVE SWITCHING WAVEFORMS

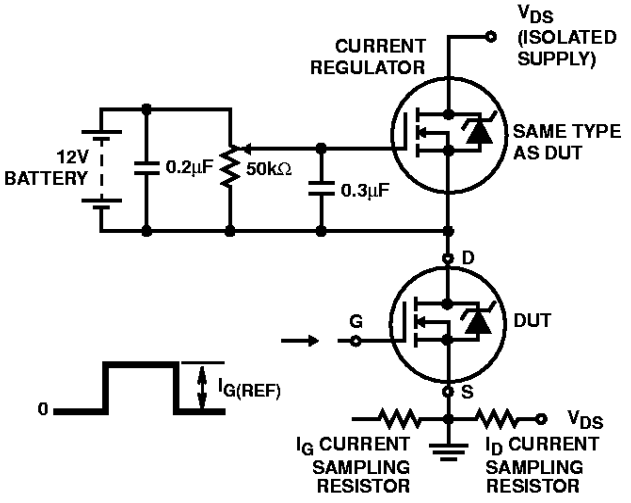


FIGURE 19. GATE CHARGE TEST CIRCUIT

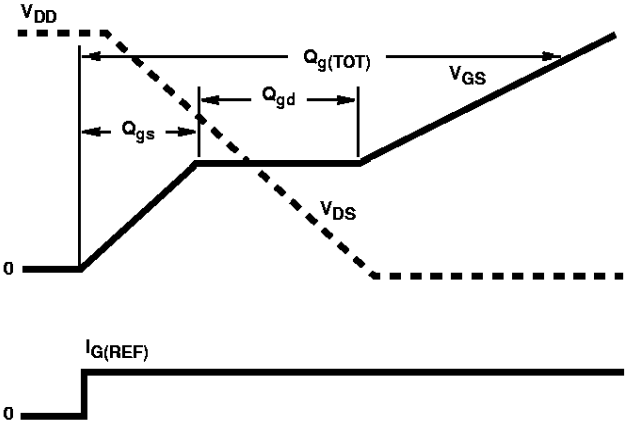


FIGURE 20. GATE CHARGE WAVEFORMS

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