FAIRCHILD SEMICONDUCTOR™

October 1987
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# CD4071BC • CD4081BC
# Quad 2-Input OR Buffered B Series Gate • Quad 2-Input AND Buffered B Series Gate

## General Description

The CD4071BC and CD4081BC quad gates are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement mode transistors. They have equal source and sink current capabilities and conform to standard B series output drive. The devices also have buffered outputs which improve transfer characteristics by providing very high gain.

All inputs protected against static discharge with diodes to $V_{DD}$ and $V_{SS}$.

## Features

- Low power TTL compatibility:
  Fan out of 2 driving 74L or 1 driving 74LS
- 5V–10V–15V parametric ratings
- Symmetrical output characteristics
- Maximum input leakage 1 μA at 15V over full temperature range

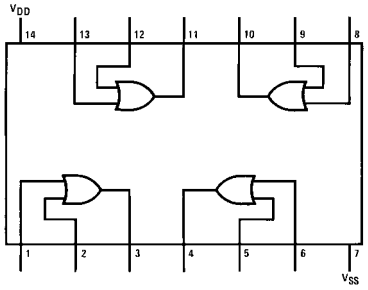
## Ordering Code:

| Order Number | Package Number | Package Description |
|---|---|---|
| CD4071BCM | M14A | 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow |
| CD4071BCN | N14A | 14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide |
| CD4081BCM | M14A | 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow |
| CD4081BCN | N14A | 14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide |

Devices are also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

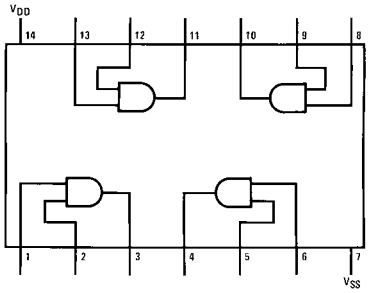
## Connection Diagrams

**CD4071B**




**Top View**

**CD4081B**

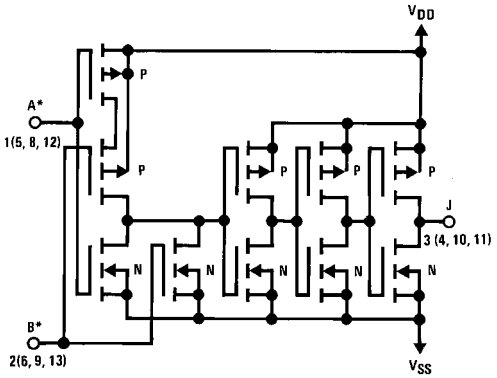


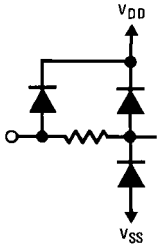

**Top View**

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## Schematic Diagrams

### CD4071B




**1/4 of device shown**

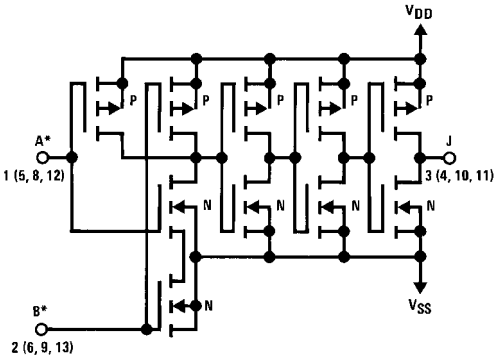
J = A + B

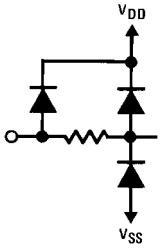
Logical "1" = HIGH

Logical "0" = LOW

*All inputs protected by standard CMOS protection circuit.

### CD4081B




**1/4 of device shown**

J = A • B

Logical "1" = HIGH

Logical "0" = LOW

All inputs protected by standard CMOS protection circuit.

## Absolute Maximum Ratings(Note 1)

(Note 2)

| | |
|---|---|
| Voltage at Any Pin | −0.5V to $V_{DD}$ +0.5V |
| Power Dissipation ($P_D$) | |
| Dual-In-Line | 700 mW |
| Small Outline | 500 mW |
| $V_{DD}$ Range | −0.5 $V_{DC}$ to +18 $V_{DC}$ |
| Storage Temperature ($T_S$) | −65°C to +150°C |
| Lead Temperature ($T_L$) | |
| (Soldering, 10 seconds) | 260°C |

## Recommended Operating Conditions

| | |
|---|---|
| Operating Range ($V_{DD}$) | 3 $V_{DC}$ to 15 $V_{DC}$ |
| Operating Temperature Range ($T_A$) | |
| CD4071BC, CD4081BC | −55°C to +125°C |

**Note 1:** "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

**Note 2:** All voltages measured with respect to $V_{SS}$ unless otherwise specified.

## DC Electrical Characteristics (Note 2)

CD4071BC/CD4081BC

| Symbol | Parameter | Conditions | −55°C | | +25°C | | | +125°C | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Typ | Max | Min | Max | |
| $I_{DD}$ | Quiescent Device | $V_{DD}$ = 5V | | 0.25 | | 0.004 | 0.25 | | 7.5 | |
| | Current | $V_{DD}$ = 10V | | 0.5 | | 0.005 | 0.5 | | 15 | µA |
| | | $V_{DD}$ = 15V | | 1.0 | | 0.006 | 1.0 | | 30 | |
| $V_{OL}$ | LOW Level | $V_{DD}$ = 5V | | 0.05 | | 0 | 0.05 | | 0.05 | |
| | Output Voltage | $V_{DD}$ = 10V $\lvert I_O \rvert$ < 1 µA | | 0.05 | | 0 | 0.05 | | 0.05 | V |
| | | $V_{DD}$ = 15V | | 0.05 | | 0 | 0.05 | | 0.05 | |
| $V_{OH}$ | HIGH Level | $V_{DD}$ = 5V | 4.95 | | 4.95 | 5 | | 4.95 | | |
| | Output Voltage | $V_{DD}$ = 10V $\lvert I_O \rvert$ < 1 µA | 9.95 | | 9.95 | 10 | | 9.95 | | V |
| | | $V_{DD}$ = 15V | 14.95 | | 14.95 | 15 | | 14.95 | | |
| $V_{IL}$ | LOW Level | $V_{DD}$ = 5V, $V_O$ = 0.5V | | 1.5 | | 2 | 1.5 | | 1.5 | |
| | Input Voltage | $V_{DD}$ = 10V, $V_O$ = 1.0V | | 3.0 | | 4 | 3.0 | | 3.0 | V |
| | | $V_{DD}$ = 15V, $V_O$ = 1.5V | | 4.0 | | 6 | 4.0 | | 4.0 | |
| $V_{IH}$ | HIGH Level | $V_{DD}$ = 5V, $V_O$ = 4.5V | 3.5 | | 3.5 | 3 | | 3.5 | | |
| | Input Voltage | $V_{DD}$ = 10V, $V_O$ = 9.0V | 7.0 | | 7.0 | 6 | | 7.0 | | V |
| | | $V_{DD}$ = 15V, $V_O$ = 13.5V | 11.0 | | 11.0 | 9 | | 11.0 | | |
| $I_{OL}$ | LOW Level Output | $V_{DD}$ = 5V, $V_O$ = 0.4V | 0.64 | | 0.51 | 0.88 | | 0.36 | | |
| | Current | $V_{DD}$ = 10V, $V_O$ = 0.5V | 1.6 | | 1.3 | 2.25 | | 0.9 | | mA |
| | (Note 3) | $V_{DD}$ = 15V, $V_O$ = 1.5V | 4.2 | | 3.4 | 8.8 | | 2.4 | | |
| $I_{OH}$ | HIGH Level Output | $V_{DD}$ = 5V, $V_O$ = 4.6V | −0.64 | | −0.51 | −0.88 | | −0.36 | | |
| | Current | $V_{DD}$ = 10V, $V_O$ = 9.5V | −1.6 | | −1.3 | −2.25 | | −0.9 | | mA |
| | (Note 3) | $V_{DD}$ = 15V, $V_O$ = 13.5V | −4.2 | | −3.4 | −8.8 | | −2.4 | | |
| $I_{IN}$ | Input Current | $V_{DD}$ = 15V, $V_{IN}$ = 0V | | −0.1 | | $-10^{-5}$ | −0.1 | | −1.0 | µA |
| | | $V_{DD}$ = 15V, $V_{IN}$ = 15V | | 0.1 | | $10^{-5}$ | 0.1 | | 1.0 | |

**Note 3:** $I_{OH}$ and $I_{OL}$ are tested one output at a time.

## AC Electrical Characteristics (Note 4)

CD4071BC $T_A$ = 25°C, Input $t_r$; $t_f$ = 20 ns, $C_L$ = 50 pF, $R_L$ = 200 kΩ, Typical temperature coefficient is 0.3%/°C

| Symbol | Parameter | Conditions | Typ | Max | Units |
|---|---|---|---|---|---|
| $t_{PHL}$ | Propagation Delay Time, | $V_{DD}$ = 5V | 100 | 250 | |
| | HIGH-to-LOW Level | $V_{DD}$ = 10V | 40 | 100 | ns |
| | | $V_{DD}$ = 15V | 30 | 70 | |
| $t_{PLH}$ | Propagation Delay Time, | $V_{DD}$ = 5V | 90 | 250 | |
| | LOW-to-HIGH Level | $V_{DD}$ = 10V | 40 | 100 | ns |
| | | $V_{DD}$ = 15V | 30 | 70 | |
| $t_{THL}$, $t_{TLH}$ | Transition Time | $V_{DD}$ = 5V | 90 | 200 | |
| | | $V_{DD}$ = 10V | 50 | 100 | ns |
| | | $V_{DD}$ = 15V | 40 | 80 | |
| $C_{IN}$ | Average Input Capacitance | Any Input | 5 | 7.5 | pF |
| $C_{PD}$ | Power Dissipation Capacity | Any Gate | 18 | | pF |

**Note 4:** AC Parameters are guaranteed by DC correlated testing.

## AC Electrical Characteristics (Note 5)

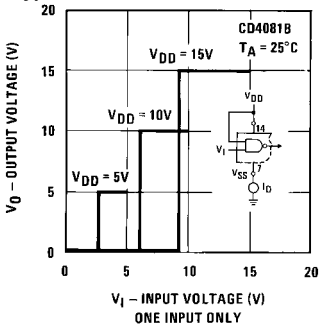
CD4081BC $T_A$ = 25°C, Input $t_r$; $t_f$ = 20 ns, $C_L$ = 50 pF, $R_L$ = 200 kΩ, Typical temperature coefficient is 0.3%/°C

| Symbol | Parameter | Conditions | Typ | Max | Units |
|---|---|---|---|---|---|
| $t_{PHL}$ | Propagation Delay Time, | $V_{DD}$ = 5V | 100 | 250 | |
| | HIGH-to-LOW Level | $V_{DD}$ = 10V | 40 | 100 | ns |
| | | $V_{DD}$ = 15V | 30 | 70 | |
| $t_{PLH}$ | Propagation Delay Time, | $V_{DD}$ = 5V | 120 | 250 | |
| | LOW-to-HIGH Level | $V_{DD}$ = 10V | 50 | 100 | ns |
| | | $V_{DD}$ = 15V | 35 | 70 | |
| $t_{THL}$, $t_{TLH}$ | Transition Time | $V_{DD}$ = 5V | 90 | 200 | |
| | | $V_{DD}$ = 10V | 50 | 100 | ns |
| | | $V_{DD}$ = 15V | 40 | 80 | |
| $C_{IN}$ | Average Input Capacitance | Any Input | 5 | 7.5 | pF |
| $C_{PD}$ | Power Dissipation Capacity | Any Gate | 18 | | pF |

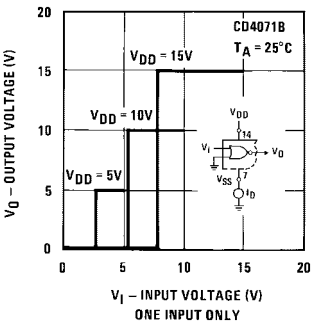
**Note 5:** AC Parameters are guaranteed by DC correlated testing.

## Typical Performance Characteristics

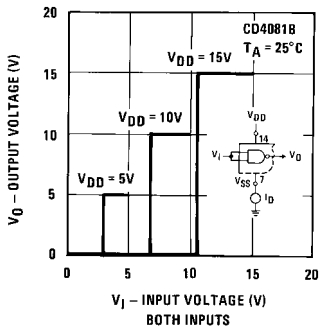
**Typical Transfer Characteristics**



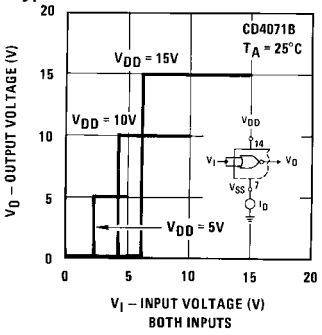

**Typical Transfer Characteristics**

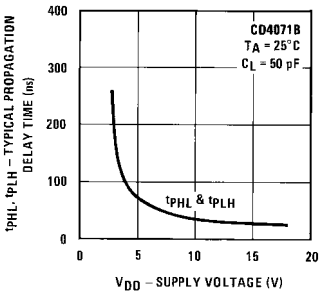



**Typical Transfer Characteristics**

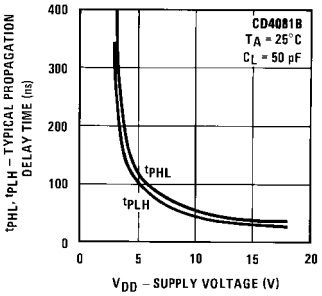


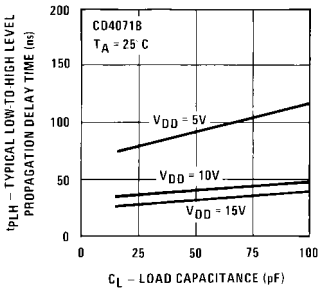

**Typical Transfer Characteristics**

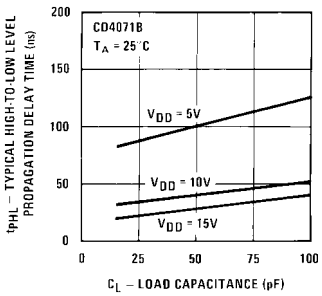


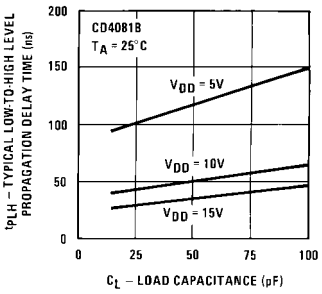



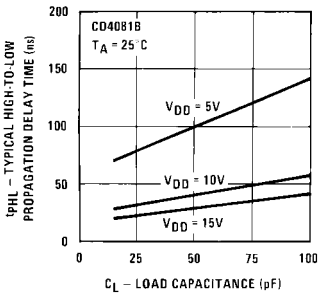
## Typical Performance Characteristics (Continued)

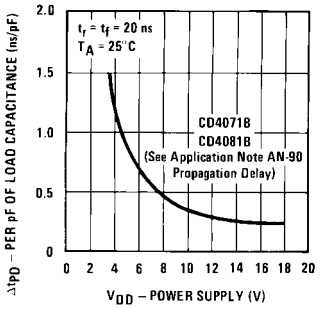


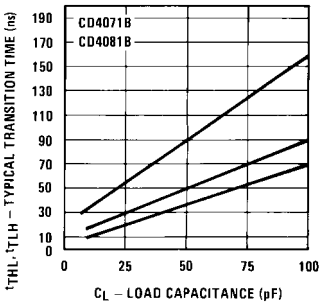



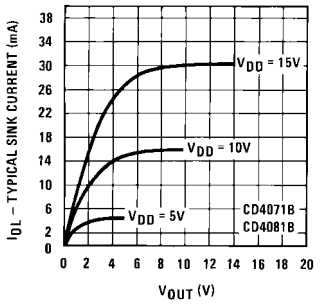



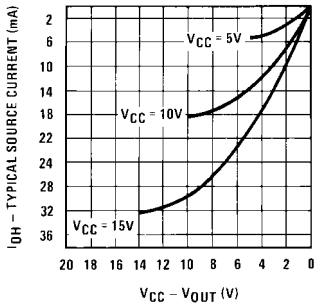



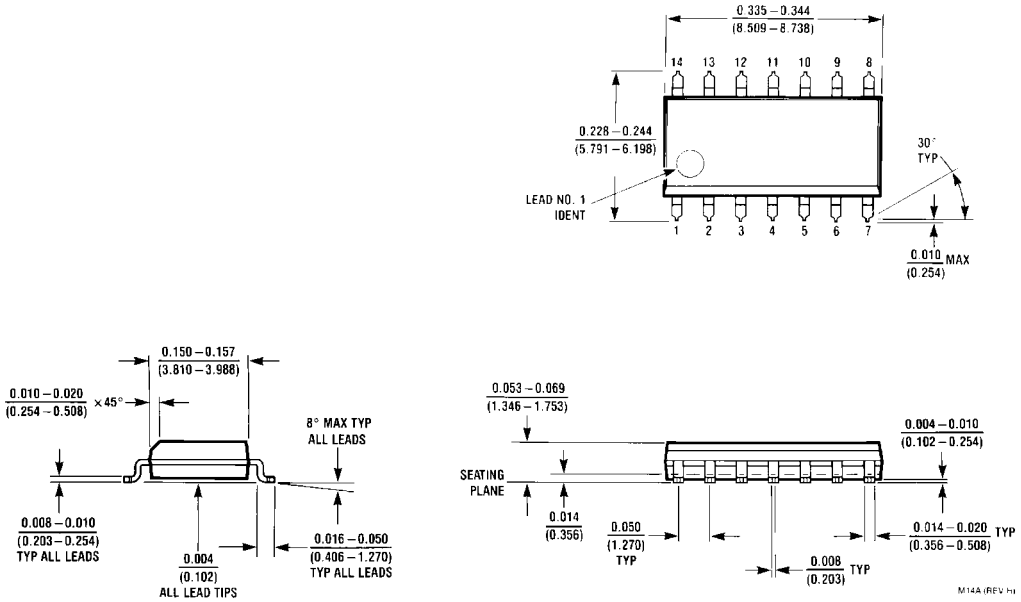



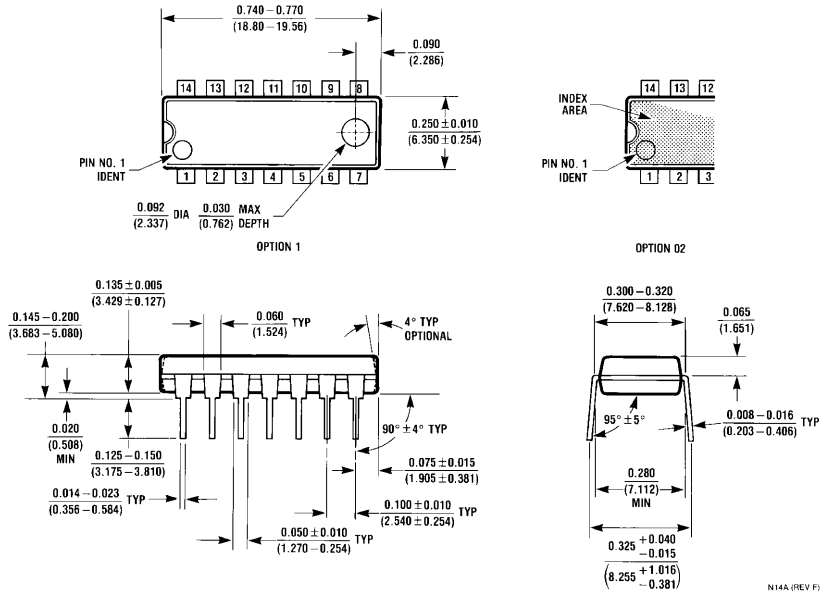



## Physical Dimensions inches (millimeters) unless otherwise noted




**14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow**
**Package Number M14A**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)




**14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide**
**Package Number N14A**

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