BTS5231-2GS

Smart High-Side Power Switch

PROFET

Two Channels, 140 m Ω

Automotive Power

Never stop thinking

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Smart High-Side Power Switch **BTS5231-2GS**
PROFET

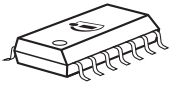
AEC Qualified RoHS

Product Summary

The BTS5231-2GS is a dual channel high-side power switch in PG-DSO-14-31 package providing embedded protective functions.

The power transistor is built by a N-channel vertical power MOSFET with charge pump. The device is monolithically integrated in Smart SIPMOS technology.

PG-DSO-14-31



Operating voltage	$V_{bb(on)}$	4.5 … 28 V
Over voltage protection	$V_{bb(AZ)}$	41 V
On-State resistance	$R_{DS(ON)}$	140 mΩ
Nominal load current (one channel active)	$I_{L(nom)}$	1.8 A
Current limitation	$I_{L(LIM)}$	8 A
Current limitation repetitive	$I_{L(SCr)}$	3 A
Standby current for whole device with load	$I_{bb(OFF)}$	2.5 µA

Basic Features

- Very low standby current
- 3.3 V and 5 V compatible logic pins
- Improved electromagnetic compatibility (EMC)
- Stable behaviour at undervoltage
- Logic ground independent from load ground
- Secure load turn-off while logic ground disconnected

Type	Ordering Code	Package
BTS5231-2GS	On request	PG-DSO-14-31

- Optimized inverse current capability
- Green product (RoHS compliant)
- AEC Qualified

Protective Functions

- Reverse battery protection without external components (GND resistor integrated)
- Short circuit protection
- Overload protection
- Multi-step current limitation
- Thermal shutdown with restart
- Thermal restart at reduced current limitation
- Overvoltage protection without external resistor
- Loss of ground protection
- Electrostatic discharge protection (ESD)

Diagnostic Functions

- Enhanced IntelliSense signal for each channel
- Enable function for diagnosis pins (IS1 and IS2)
- Proportional load current sense signal by current source
- High accuracy of current sense signal at wide load current range
- Open load detection in ON-state by load current sense
- Over load (current limitation) diagnosis in ON-state, signalling by voltage source
- Latched over temperature diagnosis in ON-state, signalling by voltage source
- Open load detection in OFF-state, signalling by voltage source

Applications

- µC compatible high-side power switch with diagnostic feedback for 12 V grounded loads
- All types of resistive, inductive and capacitive loads
- Suitable for loads with high inrush currents, so as lamps
- Suitable for loads with low currents, so as LEDs
- Replaces electromechanical relays, fuses and discrete circuits

1 Overview

The BTS5231-2GS is a dual channel high-side power switch (two times 140 mΩ) in PG-DSO-14-31 package providing embedded protective functions.

The Enhanced IntelliSense pins IS1 and IS2 provide a sophisticated diagnostic feedback signal including current sense function and open load in off state. The diagnosis signals can be switched on and off by the sense enable pin SEN.

An integrated ground resistor as well as integrated resistors at each input pin (IN1, IN2, SEN) reduce external components to a minimum.

The power transistor is built by a N-channel vertical power MOSFET with charge pump. The inputs are ground referenced CMOS compatible. The device is monolithically integrated in Smart SIPMOS technology.

1.1 Block Diagram

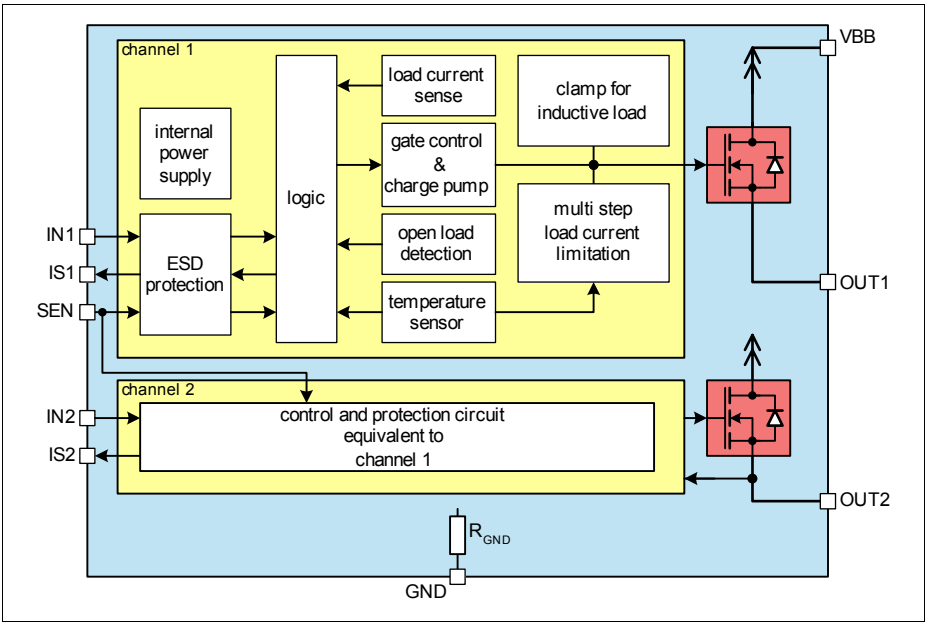


Figure 1 Block Diagram

1.2 Terms

Following figure shows all terms used in this data sheet.

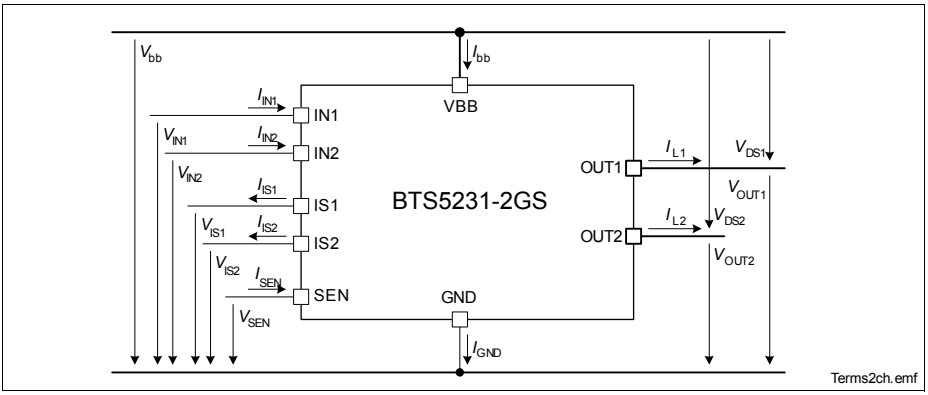


Figure 2 Terms

Symbols without channel number are channel related and valid for each channel separately.

2 Pin Configuration

2.1 Pin Assignment BTS5231-2GS

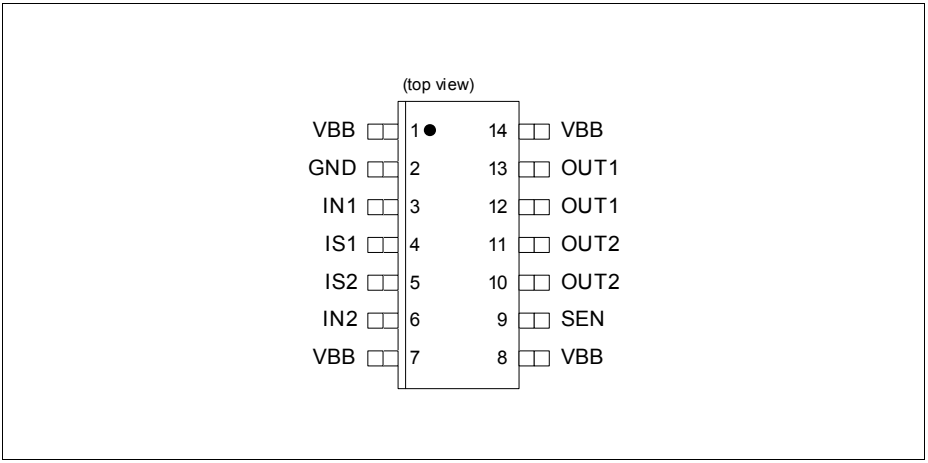


Figure 3 Pin Configuration PG-DSO-14-31

2.2 Pin Definitions and Functions

Pin	Symbol	I/O OD	Function
3	IN1	I	Input signal for channel 1
6	IN2	I	Input signal for channel 2
4	IS1	O	Diagnosis output signal channel 1
5	IS2	O	Diagnosis output signal channel 2
9	SEN	I	Sense Enable input for channel 1&2
12, 13	OUT1 [1)]	O	Protected high-side power output channel 1
10, 11	OUT2 [1)]	O	Protected high-side power output channel 2
2	GND	–	Ground connection
1, 7, 8, 14	VBB [2)]	–	Positive power supply for logic supply as well as output power supply

1) All output pins of each channel have to be connected

2) All VBB pins have to be connected

3 Electrical Characteristics

3.1 Maximum Ratings

Stresses above the ones listed here may cause permanent damage to the device. Exposure to maximum rating conditions for extended periods may affect device reliability.

T_j = 25 °C (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Test Conditions
			min.	max.		
Supply Voltage						
3.1.1	Supply voltage	V_{bb}	-16	28	V	
3.1.2	Supply voltage for full short circuit protection (single pulse) (T_j = -40 °C … 150 °C)	$V_{bb(SC)}$	0	20	V	L = 8 µH R = 0.2 Ω [1]
3.1.3	Voltage at power transistor	V_{DS}		52	V	
3.1.4	Supply Voltage for Load Dump protection	$V_{bb(LD)}$		40	V	R_I = 2 Ω [2] R_L = 12 Ω
Power Stages						
3.1.5	Load current	I_L		$I_{L(LIM)}$	A	[3]
3.1.6	Maximum energy dissipation single pulse	E_{AS}		45	mJ	[4] $I_{L(0)}$ = 2.1 A $T_{j(0)}$ = 150 °C V_{bb}=13.5V
3.1.7	Power dissipation (DC)	P_{tot}		0.9	W	[5] T_a = 85 °C $T_j \leq$ 150 °C
Logic Pins						
3.1.8	Voltage at input pin	V_{IN}	-5 -16	10	V	 $t \leq$ 2 min
3.1.9	Current through input pin	I_{IN}	-2.0 -8.0	2.0	mA	 $t \leq$ 2 min
3.1.10	Voltage at sense enable pin	V_{SEN}	-5 -16	10	V	 $t \leq$ 2 min
3.1.11	Current through sense enable pin	I_{SEN}	-2.0 -8.0	2.0	mA	 $t \leq$ 2 min

T_j = 25 °C (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Test Conditions
			min.	max.		
3.1.12	Current through sense pin	I_{IS}	-25	10	mA	–
Temperatures						
3.1.13	Junction Temperature	T_j	-40	150	°C	
3.1.14	Dynamic temperature increase while switching	ΔT_j		60	°C	
3.1.15	Storage Temperature	T_{stg}	-55	150	°C	
ESD Susceptibility						
3.1.16	ESD susceptibility HBM IN, SEN IS OUT	V_{ESD}	 -1 -2 -4	 1 2 4	kV	according to EIA/JESD 22-A 114B

1) R and L describe the complete circuit impedance including line, contact and generator impedances.

2) R_I is the internal resistance of the Load Dump pulse generator.

3) Current limitation is a protection feature. Operation in current limitation is considered as “outside” normal operating range. Protection features are not designed for continuous repetitive operation.

4) Pulse shape represents inductive switch off: $I_L(t) = I_L(0) * (1 - t / t_{pulse})$; $0 < t < t_{pulse}$.

5) Device mounted on PCB (50 mm × 50 mm × 1.5 mm epoxy, FR4) with 6 cm^2 copper heatsinking area (one layer, 70 µm thick) for V_{bb} connection. PCB is vertical without blown air.

4 Block Description and Electrical Characteristics

4.1 Power Stages

The power stages are built by a N-channel vertical power MOSFET (DMOS) with charge pump.

4.1.1 Output On-State Resistance

The on-state resistance depends on the supply voltage as well as the junction temperature T_j. **Figure 4** shows that dependencies for the typical on-state resistance $R_{DS(ON)}$. The on-state resistance in reverse polarity mode is described in **Section 4.2.2**.

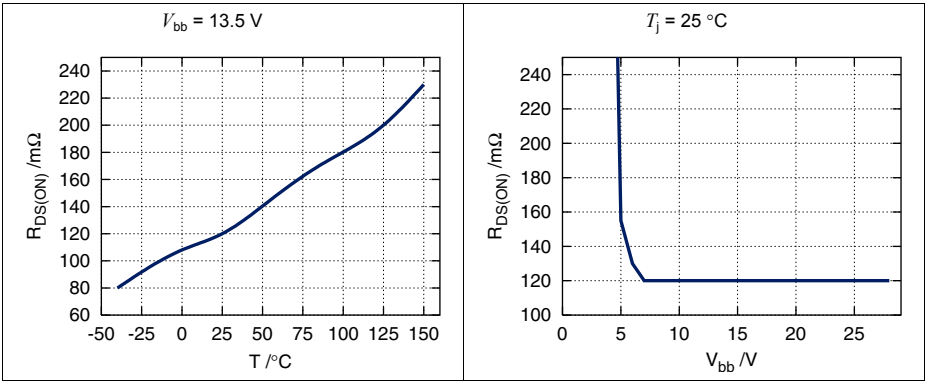


Figure 4 Typical On-State Resistance

4.1.2 Input Circuit

Figure 5 shows the input circuit of the BTS5231-2GS. There is an integrated input resistor that makes external components obsolete. The current source to ground ensures that the device switches off in case of open input pin. The zener diode protects the input circuit against ESD pulses.

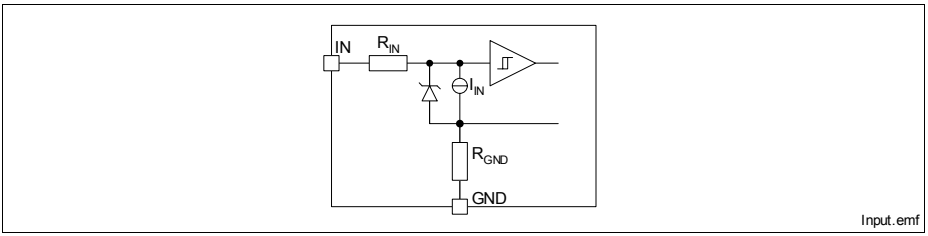


Figure 5 Input Circuit (IN1 and IN2)

A high signal at the input pin causes the power DMOS to switch on with a dedicated slope, which is optimized in terms of EMC emission.

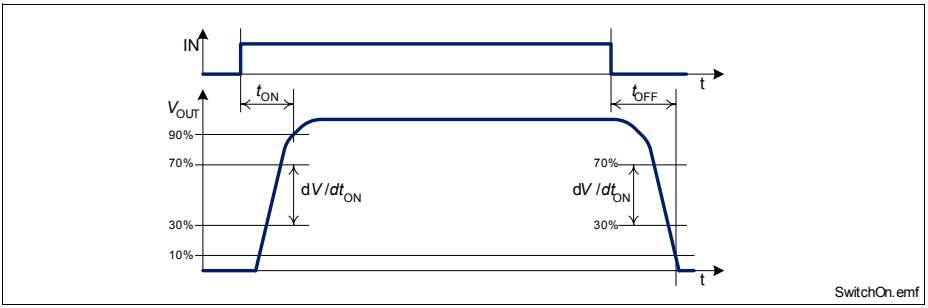


Figure 6 Switching a Load (resistive)

4.1.3 Inductive Output Clamp

When switching off inductive loads with high-side switches, the voltage V_{OUT} drops below ground potential, because the inductance intends to continue driving the current.

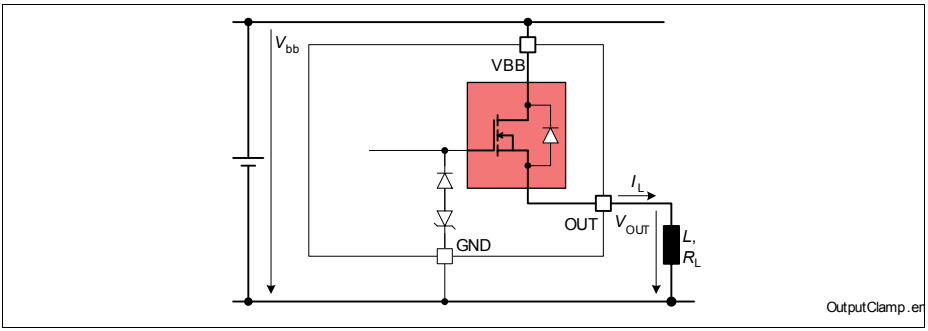


Figure 7 Output Clamp (OUT1 and OUT2)

To prevent destruction of the device, there is a voltage clamp mechanism implemented that keeps that negative output voltage at a certain level ($V_{OUT(CL)}$). See **Figure 7** and **Figure 8** for details. Nevertheless, the maximum allowed load inductance is limited.

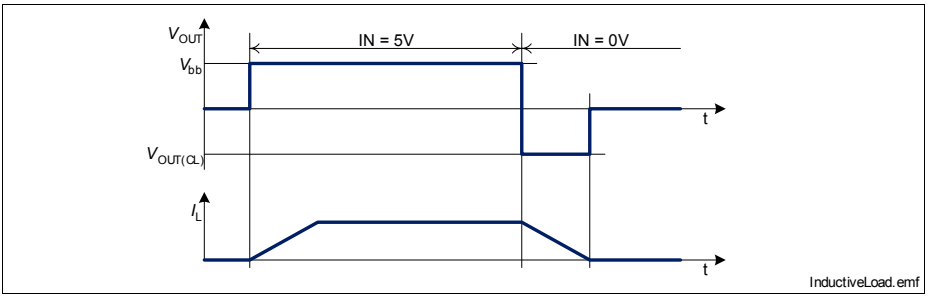


Figure 8 Switching an Inductance

Maximum Load Inductance

While demagnization of inductive loads, energy has to be dissipated in the BTS5231-2GS. This energy can be calculated with following equation:

$$E = (V_{bb} - V_{OUT(CL)}) \cdot \left[\frac{V_{OUT(CL)}}{R_L} \cdot \ln\left(1 - \frac{V_{bb}}{V_{OUT(CL)}}\right) + I_L \right] \cdot \frac{L}{R_L} \quad (1)$$

This equation simplifies under the assumption of R_L = 0:

$$E = \frac{1}{2} L I_L^2 \cdot \left(1 - \frac{V_{bb}}{V_{OUT(CL)}}\right) \quad (2)$$

The energy, which is converted into heat, is limited by the thermal design of the component. See **Figure 9** for the maximum allowed energy dissipation.

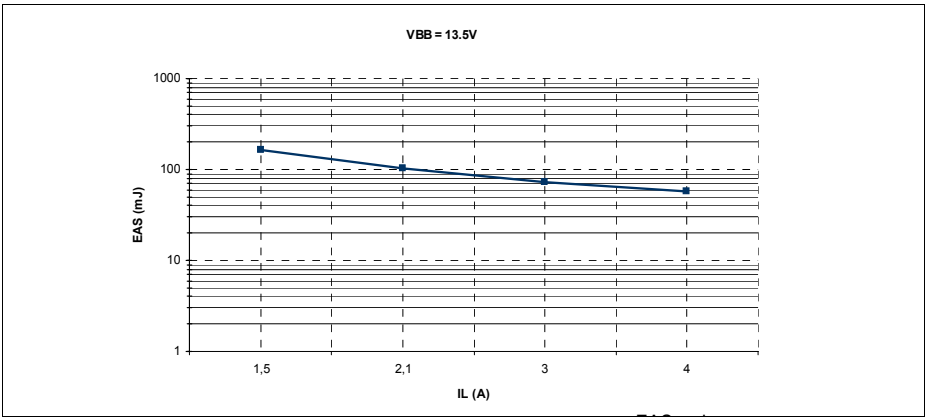


Figure 9 Maximum Energy Dissipation Single Pulse, $T_{j,Start}$ = 150 °C

4.1.4 Electrical Characteristics

V_{bb} = 9 V to 16 V, T_j = -40 °C to +150 °C (unless otherwise specified)
typical values: V_{bb} = 13.5 V, T_j = 25 °C

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
General							
4.1.1	Operating voltage	V_{bb}	4.5		28	V	V_{IN} = 4.5 V, R_L = 12 Ω, V_{DS} < 0.5 V
4.1.2	Operating current one channel active two channels active	I_{GND}		 2.0 3.8	 4.0 8.0	mA	V_{IN} = 5 V
4.1.3	Standby current for whole device with load	$I_{bb(OFF)}$		 1.5	 2.5 2.5 10	µA	V_{IN} = 0 V, V_{SEN} = 0 V, T_j = 25 °C T_j = 85 °C[1)] T_j = 150 °C
Output Characteristics							
4.1.4	On-State resistance per channel	$R_{DS(ON)}$			 140 260	mΩ	I_L = 2.5 A T_j = 25 °C T_j = 150 °C
4.1.5	Output voltage drop limitation at small load currents	$V_{DS(NL)}$		40		mV	I_L < 0.15 A
4.1.6	Nominal load current per channel one channel active two channels active	$I_{L(nom)}$	 1.8 1.3			A	T_a = 85 °C $T_j \leq$ 150 °C [2) 3)]
4.1.7	Output clamp	$V_{OUT(CL)}$	-24	-20	-17	V	I_L = 40 mA
4.1.8	Output leakage current per channel	$I_{L(OFF)}$		0.1	4.0	µA	V_{IN} = 0 V
4.1.9	Inverse current capability	$-I_{L(inv)}$		2		A	[1)]

V_{bb} = 9 V to 16 V, T_j = -40 °C to +150 °C (unless otherwise specified)
typical values: V_{bb} = 13.5 V, T_j = 25 °C

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
Thermal Resistance							
4.1.10	Junction to case	R_{thjc}			48	K/W	1)
4.1.11	Junction to ambient 2) one channel active all channels active	R_{thja}		 75 71		K/W	1) 2)
Input Characteristics							
4.1.12	Input resistance	R_{IN}	2.0	3.5	5.5	kΩ	
4.1.13	L-input level	$V_{IN(L)}$	-0.3		1.0	V	
4.1.14	H-input level	$V_{IN(H)}$	2.6		5.7	V	
4.1.15	Input hysteresis	ΔV_{IN}		0.25		V	1)
4.1.16	L-input current	$I_{IN(L)}$	3	18	75	µA	V_{IN} = 0.4 V
4.1.17	H-input current	$I_{IN(H)}$	10	38	75	µA	V_{IN} = 5 V
Timings							
4.1.18	Turn-on time to 90% V_{OUT}	t_{ON}		80	250	µs	R_L = 12 Ω, V_{bb} = 13.5 V
4.1.19	Turn-off time to 10% V_{OUT}	t_{OFF}		100	250	µs	R_L = 12 Ω, V_{bb} = 13.5 V
4.1.20	slew rate 30% to 70% V_{OUT}	dV/dt_{ON}	0.1	0.3	0.5	V/µs	R_L = 12 Ω, V_{bb} = 13.5 V
4.1.21	slew rate 70% to 30% V_{OUT}	$-dV/dt_{OFF}$	0.1	0.26	0.5	V/µs	R_L = 12 Ω, V_{bb} = 13.5 V

1) Not subject to production test, specified by design

2) Device mounted on PCB (50 mm × 50 mm × 1.5 mm epoxy, FR4) with 6 cm² copper heatsinking area (one layer, 70 µm thick) for V_{bb} connection. PCB is vertical without blown air

3) Not subject to production test, parameters are calculated from $R_{DS(ON)}$ and R_{th}

Note: Characteristics show the deviation of parameter at the given supply voltage and junction temperature. Typical values show the typical parameters expected from manufacturing.

4.2 Protection Functions

The device is fully protected by embedded protection functions. Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are neither designed for continuous nor repetitive operation.

4.2.1 Over Load Protection

The load current I_{OUT} is limited by the device itself in case of over load or short circuit to ground. There are three steps of current limitation which are selected automatically depending on the voltage V_{DS} across the power DMOS. Please note that the voltage at the OUT pin is V_{bb} - V_{DS}. Please refer to following figure for details.

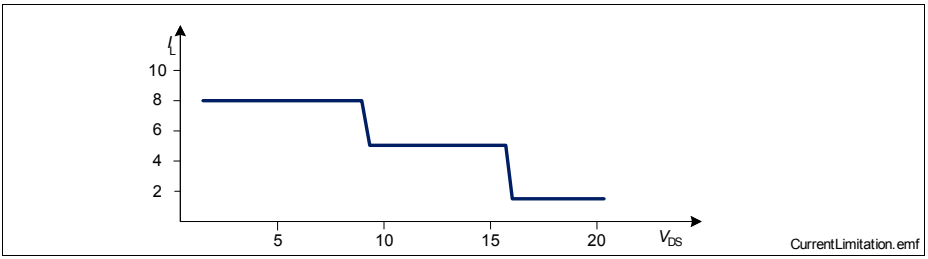


Figure 10 Current Limitation (minimum values)

Current limitation is realized by increasing the resistance of the device which leads to rapid temperature rise inside. A temperature sensor for each channel causes an overheated channel to switch off to prevent destruction. After cooling down with thermal hysteresis, the channel switches on again. Please refer to **Figure 11** for details.

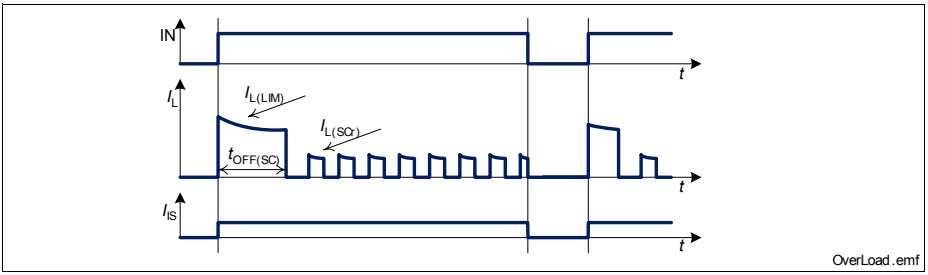


Figure 11 Shut Down by Over Temperature

In short circuit condition, the load current is initially limited to $I_{L(LIM)}$. After thermal restart, the current limitation level is reduced to $I_{L(SCr)}$. The current limitation level is reset to $I_{L(LIM)}$ by switching off the device (V_{IN} = 0 V).

4.2.2 Reverse Polarity Protection

In case of reverse polarity, the intrinsic body diode causes power dissipation. Additional power is dissipated by the integrated ground resistor. Use following formula for estimation of total power dissipation $P_{diss(rev)}$ in reverse polarity mode.

$$P_{diss(rev)} = \sum (V_{DS(rev)} \cdot I_L) + \frac{V_{bb}^2}{R_{GND}} \quad (3)$$

The reverse current through the intrinsic body diode has to be limited by the connected load. The current trough sense pins IS1 and IS2 has to be limited (please refer to maximum ratings on **Page 8**). The over-temperature protection is not active during reverse polarity.

4.2.3 Over Voltage Protection

In addition to the output clamp for inductive loads as described in **Section 4.1.3**, there is a clamp mechanism for over voltage protection. Because of the integrated ground resistor, over voltage protection does not require external components.

As shown in **Figure 12**, in case of supply voltages greater than $V_{bb(AZ)}$, the power transistor opens and the voltage across logic part is clamped. As a result, the internal ground potential rises to V_{bb} - $V_{bb(AZ)}$. Due to the ESD zener diodes, the potential at pin IN1, IN2 and SEN rises almost to that potential, depending on the impedance of the connected circuitry.

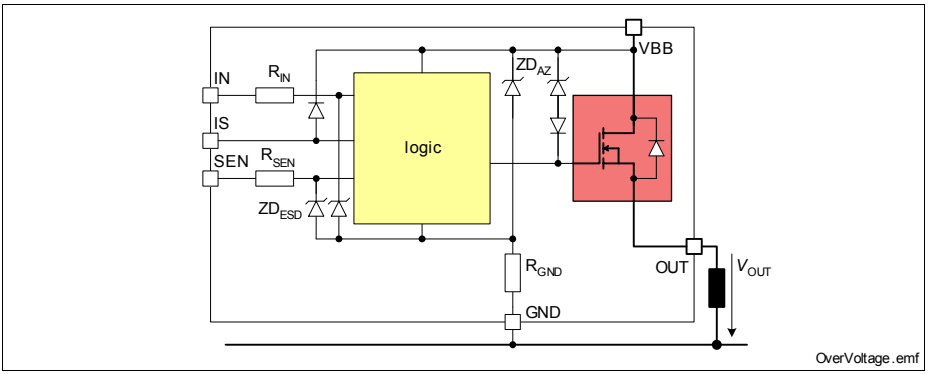


Figure 12 Over Voltage Protection

4.2.4 Loss of Ground Protection

In case of complete loss of the device ground connections, but connected load ground, the BTS5231-2GS securely changes to or keeps in off state.

4.2.5 Electrical Characteristics

V_{bb} = 9 V to 16 V, T_j = -40 °C to +150 °C (unless otherwise specified)
typical values: V_{bb} = 13.5 V, T_j = 25 °C

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
Over Load Protection							
4.2.1	Load current limitation	$I_{L(LIM)}$	8 5 1.6		16 10 6	A	V_{DS} = 7 V V_{DS} = 14 V V_{DS} = 28 V 1) 2)
4.2.2	Repetitive short circuit current limitation	$I_{L(SCr)}$		3		A	$T_j = T_{j(SC)}$ 2)
4.2.3	Initial short circuit shut down time	$t_{OFF(SC)}$		0.5		ms	T_{jStart} = 25 °C 2) R_{thja} = 40 K/W
4.2.4	Thermal shut down temperature	$T_{j(SC)}$	150	170 2)		°C	
4.2.5	Thermal hysteresis	ΔT_j		10		K	
Reverse Battery							
4.2.6	Drain-Source diode voltage (V_{OUT} > V_{bb})	$-V_{DS(rev)}$			700	mV	I_L = -1.6 A, V_{bb} = -13.5 V, T_j = 150 °C
4.2.7	Reverse current through GND pin	$-I_{GND}$		65		mA	V_{bb} = -13.5 V 2)
Ground Circuit							
4.2.8	Integrated Resistor in GND line	R_{GND}	115 200	220	350 350	Ω Ω	T_j < 150 °C T_j = 150 °C
Over Voltage							
4.2.9	Overvoltage protection	$V_{bb(AZ)}$	41	47	53	V	I_{bb} = 2 mA
Loss of GND							
4.2.10	Output current while GND disconnected	$I_{L(GND)}$			2	mA	I_{IN} = 0, 2) 3) I_{SEN} = 0, I_{IS} = 0, I_{GND} = 0

1) Please note, that an external forced V_{DS} must not exceed V_{bb} + $|V_{OUT(CL)}|$

2) Not subject to production test, specified by design

3) No connection at these pins

4.3 Diagnosis

For diagnosis purpose, the BTS5231-2GS provides an Enhanced IntelliSense signal at pins IS1 and IS2. This means in detail, the current sense signal I_{IS}, a proportional signal to the load current (ratio k_{ILIS} = I_L / I_{IS}), is provided as long as no failure mode (see **Table 1**) occurs. In case of a failure mode, $V_{IS(fault)}$ is fed to the diagnosis pin.

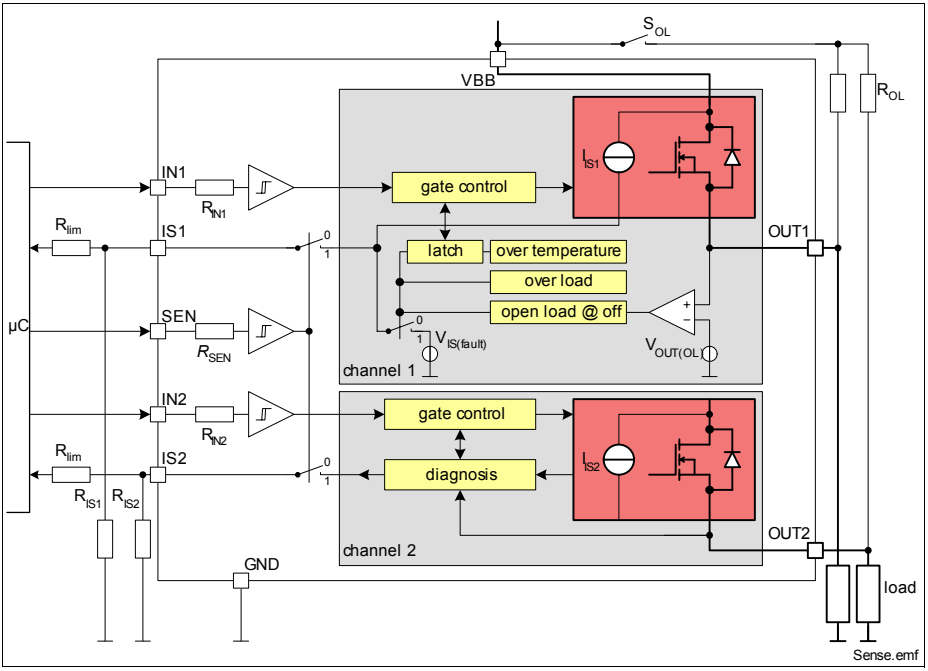


Figure 13 Block Diagram: Diagnosis

Table 1 Truth Table [1)]

Operation Mode	Input Level	Output Level	Diagnostic Output	
			SEN = H	SEN = L
Normal Operation (OFF)	L (OFF-State)	GND	Z	Z
Short Circuit to GND		GND	Z	Z
Over-Temperature		Z	Z	Z
Short Circuit to V_{bb}		V_{bb}	V_{IS} = $V_{IS(fault)}$	Z
Open Load		< $V_{OUT(OL)}$ > $V_{OUT(OL)}$	Z V_{IS} = $V_{IS(fault)}$	Z Z

Table 1 Truth Table (cont'd)[1)]

Operation Mode	Input Level	Output Level	Diagnostic Output	
			SEN = H	SEN = L
Normal Operation (ON)	H (ON-State)	~V_{bb}	$I_{IS} = I_L / k_{ILIS}$	Z
Current Limitation		< V_{bb}	$V_{IS} = V_{IS(fault)}$	Z
Short Circuit to GND		~GND	$V_{IS} = V_{IS(fault)}$	Z
Over-Temperature		Z	$V_{IS} = V_{IS(fault)}$	Z
Short Circuit to V_{bb}		V_{bb}	$I_{IS} < I_L / k_{ILIS}$	Z
Open Load		V_{bb}	Z	Z

1) L = Low Level, H = High Level, Z = high impedance, potential depends on leakage currents and external circuit

4.3.1 ON-State Diagnosis

The standard diagnosis signal is a current sense signal proportional to the load current. The accuracy of the ratio ($k_{ILIS} = I_L / I_{IS}$) depends on the temperature. Please refer to **Figure 14** for details. Usually a resistor R_{IS} is connected to the current sense pin. It is recommended to use sense resistors R_{IS} > 500 Ω. A typical value is 4.7 kΩ

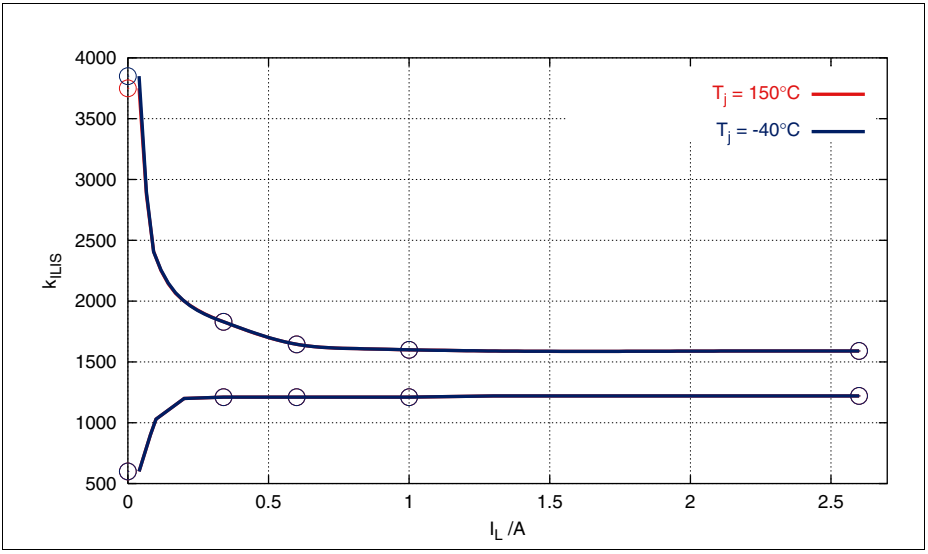


Figure 14 Current Sense Ratio k_{ILIS}[1)]

1) The curves show the behavior based on characterization data. The marked points are guaranteed in this Data Sheet in **Section 4.3.4** (Position **4.3.6**).

Details about timings between the diagnosis signal I_{IS} and the output voltage V_{OUT} and load current I_L in ON-state can be found in **Figure 15**.

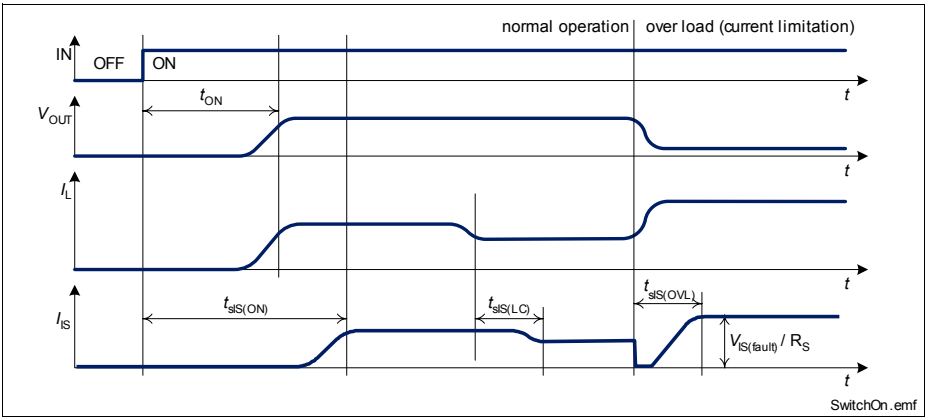


Figure 15 Timing of Diagnosis Signal in ON-state

In case of over-load as well as over-temperature, the voltage $V_{IS(fault)}$ is fed to the diagnosis pins as long as the according input pin is high. This means, even if the overload disappears after the first thermal shutdown or when the device keeps switching on and off in over-load condition (thermal toggling), the diagnosis signal ($V_{IS(fault)}$) is constantly available. Please refer to **Figure 16** for details. Please note, that if the overload disappears before the first thermal shutdown, the diagnosis signal ($V_{IS(fault))}$ may remain for approximately up to 300 µs longer than the duration of the overload.

As a result open load and over load including over temperature can be differentiated in ON-state.

Consideration must be taken in the selection of the sense resistor in order to distinguish nominal currents from the overload/short circuit fault state. A potential of 5 V at the sense pin can be achieved with a big sense resistor even with currents being much smaller than the current limitation.

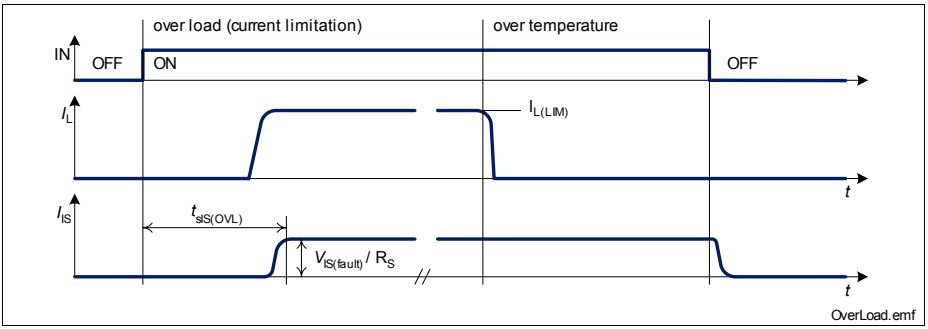


Figure 16 Timing of Diagnosis Signal in Over Load Condition

4.3.2 OFF-State Diagnosis

Details about timings between the diagnosis signal I_{IS} and the output voltage V_{OUT} and load current I_L in OFF-state can be found in **Figure 17**. For open load diagnosis in OFF-state an external output pull-up resistor (R_{OL}) is necessary.

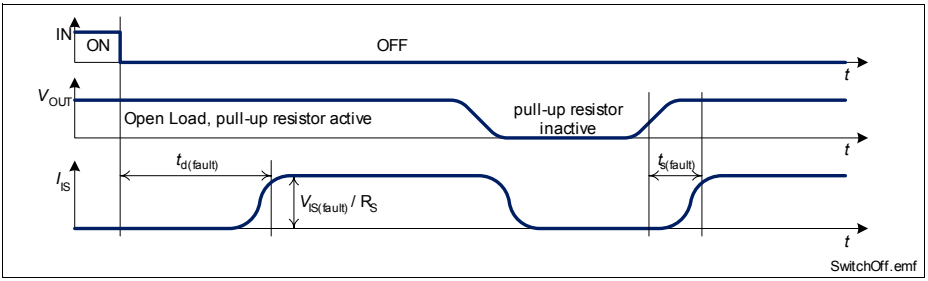


Figure 17 Timing of Diagnosis Signal in OFF-State

For calculation of the pull-up resistor, just the external leakage current $I_{leakage}$ and the open load threshold voltage $V_{OUT(OL)}$ has to be taken into account.

$$R_{OL} = \frac{V_{bb(min)} - V_{OUT(OL,max)}}{I_{leakage}} \quad (4)$$

$I_{leakage}$ defines the leakage current in the complete system e.g. caused by humidity. There is no internal leakage current from out to ground at BTS5231-2GS. $V_{bb(min)}$ is the minimum supply voltage at which the open load diagnosis in off state must be ensured. To reduce the stand-by current of the system, an open load resistor switch (S_{OL}) is recommended.

4.3.3 Sense Enable Function

The diagnosis signals have to be switched on by a high signal at sense enable pin (SEN). See **Figure 18** for details on the timing between SEN pin and diagnosis signal I_{IS}. Please note that the diagnosis is disabled, when no signal is provided at pin SEN.

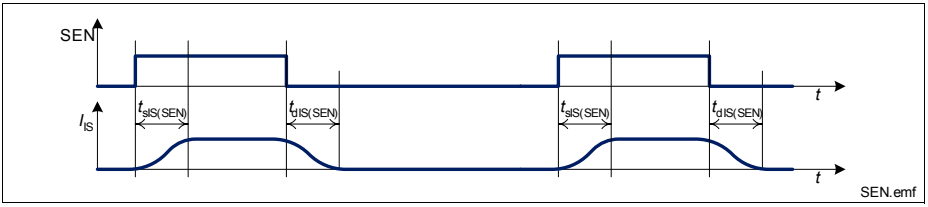


Figure 18 Timing of Sense Enable Signal

The SEN pin circuit is designed equal to the input pin. Please refer to **Figure 5** for details. The resistors R_{lim} are recommended to limit the current through the sense pins IS1 and IS2 in case of reverse polarity and over-voltage. Please refer to maximum ratings on **Page 8**. The stand-by current of the BTS5231-2GS is minimized, when both input pins (IN1 and IN2) and the sense enable pin (SEN) are on low level.

4.3.4 Electrical Characteristics

V_{bb} = 9 V to 16 V, T_j = -40 °C to +150 °C, V_{SEN} = 5 V (unless otherwise specified)
typical values: V_{bb} = 13.5 V, T_j = 25 °C

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
General Definition							
4.3.1	Diagnostics signal in failure mode	$V_{IS(fault)}$	5		9	V	V_{IN} = 0 V V_{OUT} = V_{bb} I_{IS} = 1 mA
4.3.2	Diagnostics signal current limitation in failure mode	$I_{IS(LIM)}$	3			mA	V_{IN} = 0 V V_{OUT} = V_{bb}
Open Load at OFF-State							
4.3.3	Open load detection threshold voltage	$V_{OUT(OL)}$	1.6	2.8	4.4	V	
4.3.4	Sense signal invalid after negative input slope	$t_{d(fault)}$			1.2	ms	V_{IN} = 5 V to 0 V V_{OUT} = V_{bb}
4.3.5	Fault signal settling time	$t_{s(fault)}$			200	µs	V_{IN} = 0 V V_{OUT} = 0 V to > $V_{OUT(OL)}$ I_{IS} = 1 mA
Load Current Sense							
4.3.6	Current sense ratio	k_{ILIS}					V_{IN} = 5 V
	I_L = 0.04 A		600	2000	3850		T_j = -40 °C
	I_L = 0.34 A		1210	1490	1830		
	I_L = 0.6 A		1210	1416	1645		
	I_L = 1.0 A		1210	1410	1600		
	I_L = 2.6 A		1220	1405	1590		
	I_L = 0.04 A		600	1950	3750		T_j = 150 °C
	I_L = 0.34 A		1210	1490	1830		
	I_L = 0.6 A		1210	1416	1645		
	I_L = 1.0 A		1210	1410	1600		
	I_L = 2.6 A		1220	1405	1590		
4.3.7	Current sense voltage limitation	$V_{IS(LIM)}$	5.0	5.9	7.5	V	I_{IS} = 0.5 mA I_L = 2.6 A

V_{bb} = 9 V to 16 V, T_j = -40 °C to +150 °C, V_{SEN} = 5 V (unless otherwise specified)
typical values: V_{bb} = 13.5 V, T_j = 25 °C

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
4.3.8	Current sense leakage/offset current	$I_{IS(LH)}$			3.5	µA	V_{IN} = 5 V I_L = 0 A
4.3.9	Current sense leakage, while diagnosis disabled	$I_{IS(dis)}$			1	µA	V_{SEN} = 0 V I_L = 2.6 A
4.3.10	Current sense settling time to I_{IS} static ±10% after positive input slope	$t_{sIS(ON)}$			300	µs	V_{IN} = 0 V to 5 V I_L = 1.6 A 1)
4.3.11	Current sense settling time to I_{IS} static ±10% after change of load current	$t_{sIS(LC)}$			50	µs	V_{IN} = 5 V I_L = 1 A to 0.6 A 1)
Over Load in ON-State							
4.3.12	Over load detection current	$I_{L(OVL)}$	4		$I_{L(LIM)}$	A	V_{IN} = 5 V V_{IS} = $V_{IS(fault)}$ 1)
4.3.13	Sense signal settling time in overload condition	$t_{sIS(OVL)}$			200	µs	V_{OUT} = 2 V V_{IN} = 0 V to 5 V
Sense Enable							
4.3.14	Input resistance	R_{SEN}	2.0	3.5	5.5	kΩ	
4.3.15	L-input level	$V_{SEN(L)}$	-0.3		1.0	V	
4.3.16	H-input level	$V_{SEN(H)}$	2.6		5.7	V	
4.3.17	L-input current	$I_{SEN(L)}$	3	18	75	µA	V_{SEN} = 0.4 V
4.3.18	H-input current	$I_{SEN(H)}$	10	38	75	µA	V_{SEN} = 5 V
4.3.19	Current sense settling time after positive SEN slope	$t_{sIS(SEN)}$		3	25	µs	V_{SEN} = 0 V to 5 V V_{IN} = 0 V V_{OUT} > $V_{OUT(OL)}$
4.3.20	Current sense deactivation time after negative SEN slope	$t_{dIS(SEN)}$			25	µs	V_{SEN} = 5 V to 0 V I_L = 2 A R_S = 5 kΩ 1)

1) Not subject to production test, specified by design

5 Package Outlines BTS5231-2GS

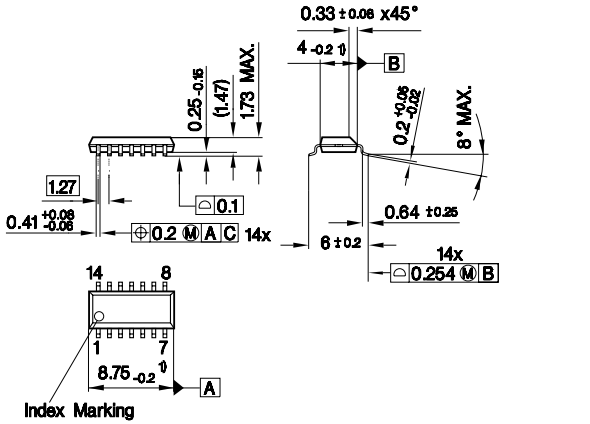


Figure 19 PG-DSO-14-31 (Plastic Dual Small Outline Package)

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/ JEDEC J-STD-020).

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6 Revision History

Version	Date	Changes
V1.1	2007-06-14	Chapter 4.3.3 Before : Please note that the diagnosis is **en**abled, when no signal is provided at pin SEN After : Please note that the diagnosis is **dis**abled, when no signal is provided at pin SEN
V1.0	2007-04-17	Creation of the green datasheet. Delta sheet to the grey BTS5231GS datasheet of December the 19th 2005 version 1.0 : Parameter 3.1.6 : Change to 45mJ at 13.5V Figure 9 new. Parameter 4.1.7 : Change to -24V min, -17V max • Modification of the green logos (suppression in the package outline and addition on the overview page 4.3.11: Test conditions: Typo corrected

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