Errata (All Date Codes)

- **Releasing Reset Condition without Clock**
- **Incorrect Channel Changes in Free Running Mode**
- **32 kHz Oscillator may Fail at Higher Voltages**
- **Error in Half Carry Flag**
- **Error in Writing Reset Status Bits**
- **Wake-up from Sleep Executes Instructions before the Interrupt is Serviced**
- **The SPI Can Send Wrong Byte**
- **Serial Programming at Voltages below 3.0V**
- **Wake-up from Power-save without Global Interrupt Enabled**
- **UART Loses Synchronization if RXD Line is Low when UART Receive is Disabled**

10. Releasing Reset Condition without Clock

If an external reset or a watchdog reset occurs while the clock is stopped and reset is released before the clock is restarted, the internal reset will timeout after the start-up delay which is independent of the external clock. If no external clock pulses are present in the period when internal reset is active, the reset does correctly cause tri-stating of the I/O while the reset is held. However, if the internal reset is released before the clock starts running, the part does not clear I/O registers, nor sets PC to 0x00. Here, stopping the clock refers to gating the external clock input. Power-down or Power-save mode do not have this issue.

Problem Fix/Workaround

Make sure the clock is running whenever an external reset can be expected. If the Watchdog is used, never stop an external clock.

9. Incorrect Channel Changes in Free Running Mode

If the ADC operates in Free Running Mode and channels are changed by writing to ADMUX shortly after the ADC Interrupt Flag (ADIF in ADCSR) is set, the new setting in ADMUX may affect the ongoing conversion.

Problem Fix/Workaround

Use Single Conversion Mode when scanning channels, or avoid changing ADMUX until at least 0.5 ADC clock cycles after ADIF goes high.

8. 32 kHz Oscillator may Fail at Higher Voltages

When using an external 32 kHz crystal as asynchronous clock source for Timer2, the timer may count incorrectly at voltages above 4.0V.

Problem Fix/Workaround

Keep the supply voltage below 4.0V when clocking Timer2 from an external crystal.

7. Error in Half Carry Flag

The half carry flag is undefined after executing the commands “ror”, “asr” and “lsr”.

Problem Fix/Workaround

Do not use the half carry flag value after executing the above instructions.

8-bit AVR® Microcontroller with 8K Bytes of In-System Programmable Flash

AT90S/LS8535 Rev. E Errata Sheet

Rev. 1657C–11/01

6. Error in Writing Reset Status Bits

The EXTRF flag in MCUSR will be cleared when clearing the PORF-flag. The flag does not get cleared by writing a “0” to it.

Problem Fix/Workaround

Finish the test of both flags before clearing any of them. Clear both flags simultaneously by writing “0” to both PORF and EXTRF in MCUCR.

5. Wake-up from Sleep Executes Instructions before the Interrupt is Serviced

When waking up from Power-save, some instructions are executed before the interrupt is called. If the device is woken up by an external interrupt, 2 instruction cycles are executed. If it is woken up by the asynchronous timer, 3 instructions are executed before the interrupt.

Problem Fix/Workaround

Make sure that the first two or three instructions following sleep are not dependent on the executed interrupt.

4. The SPI Can Send Wrong Byte

If the SPI is in Master mode, it will restart the old transfer if new data is written on the same clock edge as the previous transfer is finished.

Problem Fix/Workaround

When writing to the SPI, first wait until it is ready, then write the byte to transmit.

3. Serial Programming at Voltages below 3.0V

At voltages below 3.0V, serial programming might fail.

Problem Fix/Workaround

Keep V_{CC} at 3.0V or higher during In-System Programming.

2. Wake-up from Power-save without Global Interrupt Enabled

When an asynchronous timer interrupt is used to wake up the part from Power-save, the part will wake up even if global interrupts are disabled.

Problem Fix/Workaround

No workaround necessary.

1. UART Loses Synchronization if RXD Line is Low when UART Receive is Disabled

The UART will detect a UART start bit and start reception even if the UART is not enabled. If this occurs, the first byte after re-enabling the UART will be corrupted.

Problem Fix/Workaround

Make sure that the RX line is high at start-up and when the UART is disabled. An external RS-232 level converter keeps the line high during start-up.

Significant Datasheet Changes

Revision D and older contained an errata allowing PORTD register to change the state of the output compare value of Timer/Counter1. This error is described as errata #7 in AT90S/LS8535 revision D erratasheet. Because of the high likelihood of users to experience this error, the erratic behaviour was also described in the databook.

From revision E this errata is corrected. Writing to PORTD5 and PORTD4 will not set the OC1A and OC1B respectively and the datasheet has been changed to describe the correct device behaviour (datasheet revision 1041H or later).

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